In re Appln. of Nick P. DiVittorio
Application No. 09/449,912

REMARKS

The Office Action dated March 20, 2003, and the references cited therein have been carefully considered. Claims 1-26 are presently pending. No claims currently stand allowed. Claims 1, 8, 20, 23, 25 and 26 have been amended to remedy clerical errors and ensure the clarity of the claims. None of the amendments are intended to impose further limitations on the claimed invention. In view of the remarks set forth herein below, the pending claims 1-26 are patentable over the prior art presently known to Applicant. Accordingly, Applicant requests favorable reconsideration of the previous rejection of the now pending claims. Please charge any fee deficiencies to Deposit Account No. 12-1216.

Summary of the Claim Rejections

The following identifies the authority and prior art applied to the identified claims for each rejection of the claims set forth in the Office Action dated March 20, 2003.

1. **Sections 2-3**: Claims 7 and 19 are rejected under Section 112, paragraphs 1 and 2 as not being enabled and indefinite.

2. **Section 4**: Claim 26 is rejected under Section 102(e) as anticipated by Dailey U.S. Pat. No. 6,330,483 (filed May 7, 1999 and issued Dec. 11, 2001).

3. **Sections 5-9**: Claims 1-2, 5, 13-14, 17 and 25 are rejected under Section 103(a) as obvious over Dailey in view of Daggett et al. U.S. Pat. No. 4,786,847.

4. **Sections 10-11**: Claims 3-4 and 15-16 are rejected under Section 103(a) as obvious over Dailey in view of Daggett et al. and Morshedi et al. U.S. Pat. No. 5,481,716.

5. **Sections 12-21**: Claims 6, 8-12, and 20-24 are rejected under Section 103(a) as obvious over Dailey in view of Daggett et al. and McManus et al. U.S. Pat. No. 4,788,647.

6. **Section 22**: Claims 7 and 19 are rejected under Section 103(a) as obvious over the Dailey in view of Daggett et al. and Westergren et al. U.S. Pat. No. 5,423,076.

Applicant traverses the grounds for each and every rejection for the reasons set forth herein below.

Turning initially to the Section 112 rejections, **sections 2-3** of the Office Action object, on enablement and indefiniteness grounds, to the recitation of "ratio block" in claims 7 and 19. Applicant traverses both the "enablement" and "indefiniteness" rejections. In particular, the Specification refers to "well known" input, output, PID, and *ratio* blocks (see,

Specification at page 6, line 20). The ratio block was a known regulatory control block in the area of process control that receives as inputs (1) a measurement signal and (2) a ratio. The ratio block output is equal to the measurement multiplied by the ratio. Furthermore, Applicant requests withdrawal of this rejection in view of the Office Action's own identification of a version of the known ratio block in Westergren – cited in the rejection of claims 7 and 19 as obvious. In the event that this rejection is not withdrawn, Applicant stands ready to provide further publications that existed at the time of filing describing the known "ratio block" recited in claims 7 and 19.

Applicant traverses the rejection, at **section 4** of the Office Action, of claim 26 under Section 102(e) as anticipated by Dailey U.S. Pat. No. 6,330,483. As an initial matter, in responding to this Office Action, Applicant reserves the right (and stands ready if necessary) to swear behind the Dailey reference. However, for at least the reasons set forth herein below, the Dailey reference, even if deemed prior art, would not render Applicant's claim 26 unpatentable since Dailey lacks a number of the recited elements.

The invention recited in claim 26 is directed to a multi-level multivariable industrial process control program execution framework for an industrial control processor. The recited *multi-level* control program execution framework thus includes at least two distinct levels of control program *execution*. A first cyclically executed sequence of instructions, executed at a relatively lower priority, is repeated according to a first *configurable* repetition period (e.g., every 5 seconds) to render setpoints for regulatory control blocks based upon a set of input variables. In the illustrative embodiment of the invention, the first cyclically executed sequence of instructions, executed at a relatively lower priority, corresponds to the multivariable control application 138. The values (including setpoint values) rendered by the control application 138 (described as a linear program that operates upon potentially hundreds of input values) are generally computationally intensive, but generally less time-critical. The control processor executes the control application 138 after higher priority tasks have been executed by the control processor. Furthermore, the repetition cycle of the multivariable control application 138 is configurable – thus enabling a supervisor (e.g., a human, an automated supervisory monitor program) to adjust the repetition period according to needs/processing load.

The invention recited in claim 26 also includes a second cyclically executed sequence of instructions. The second cyclically executed sequence of instructions is executed at a higher execution priority level (e.g., as an interrupt-invoked foreground task) than the first cyclically executed instructions. The second cyclically executed sequence is repeated according to a second repetition period. In the illustrative embodiment, the second cyclically executed sequence includes the regulatory control blocks that carry out the interface between the control processor and the field devices that carry out the control instructions (e.g., setpoints) rendered by the multivariable control application 138. The regulatory control blocks are executed after an interrupt is generated after a relatively short period of time (e.g., every half second) in comparison to the first repetition period of the multivariable control application. For at least the reasons expressed herein below, Applicant asserts that the invention recited in claim 26, including the first and second cyclically executed sequences of instructions, is neither disclosed nor suggested by the Dailey patent.

The Dailey patent, upon which the rejection of claim 26 is based, discloses a flight control system for a flying object (e.g., an airplane, rocket, missile, etc.). The Dailey patent discloses a control system including potentially multiple command channels – the output signals that control rudder, aileron, flap, etc. positions on the flying object. The Dailey patent first discloses a way for eliminating integrator windup (when a controlled element cannot change as quickly as desired by the control system). The Dailey patent also discloses a control method including assigning priorities to *output channel values* for controlling flight.

However, Dailey does not disclose carrying out control through *execution of the sequences of instructions* having differing priorities recited in claim 26. Instead, Dailey's reference to "priorities" concerns, as explained at col. 18, lines 22-41, control affecters. The primary control affecters are used first, then the secondary control affecters are used when the primary control affecters saturate. This teaching is reinforced at column 19, lines 46-64. Thus, Dailey discloses prioritization of control affecters (output channels) rather than prioritizing execution of the two distinct sets of cyclically executing program sequences described in claim 26.

Dailey also appears to disclose a single cyclically executed control loop that calculates both the primary and secondary channel values. Dailey, at col. 39, lines 1-3 refers to beginning

a new iteration cycle. Thus, at each iteration cycle, the controller calculates new values for all channels (both primary and secondary).

Dailey does not include a number of elements specifically recited in independent claim 26. As an initial matter, the Office Action does not identify any teaching within Dailey of a "first *configurable* repetition period." The Office Action cites disclosure of an iteration cycle (at col. 39, lines 1-3). However, the disclosure of beginning a new iteration cycle does not mean that a repetition period has been established or that the duration of the repetition period is configurable. Nor does the Office Action identify a teaching within the Dailey reference that a first repetition period is changed through a configuration request.

Furthermore, there is no suggestion in Dailey to make such modification to Dailey's disclosed control system. The control system cycle load in Dailey is not likely to change in view of its intended environment (i.e., a particular controlled flying object). Instead of being a general-purpose control system, Dailey discloses systems created specifically for a particular use (e.g., controlling a missile's flight path, an airplane's flight control surfaces, etc.). Thus, in the case of Dailey, a repetition period (if such fixed period even exists in Dailey) is established during programming of the control system and there is no suggestion in Dailey that the programmed repetition period is somehow changed through later configuration.

The Office Action does not identify the presence of distinct first *and* second cyclically executed sequences of instructions as recited in claim 26. The recited invention identifies two distinct cyclically executed instruction sequences operating at differing levels of priority and according to distinctly designated repetition periods. It is Applicant's understanding that Dailey discloses a single control sequence that is executed on a repeating basis to render values for the signal channels according to the L1 Optimization Algorithm.

Rather than identify two distinct execution levels in the Dailey patent, the Office Action references signal channels having differing priority levels. See, col. 18, lines 22-41 and col. 19, lines 46-64. The priority levels are assigned to the signal channels as part of the optimization of the control of the flying object. Primary channels are given higher importance than secondary channels during optimization. Nowhere does Dailey disclose or suggest that the signal channel values are rendered by program sequences that operate at differing execution priority levels. Furthermore, since the channel values are calculated by a single control sequence, then there cannot be two distinctly designated control sequences.

In addition to addressing the above shortcomings of Dailey's disclosure identified above, in the event that the rejection of claim 26 is not withdrawn, Applicant requests identification, within Dailey, of "a set of instructions for calculating a setpoint value for a process control variable" (in the first cyclically executed sequence of instructions). The Office Action references Dailey, at col. 15, lines 50-65 as disclosing such setpoint. However, nothing in Dailey suggests that the output variables identified in the equations are setpoint values. In the event that this rejection is not withdrawn, Applicant requests an explanation of how Dailey discloses a setpoint value for a process control variable at col. 15, lines 50-65.

Applicant traverses the rejection, at **sections 5-9** of the Office action, of claims 1-2, 5, 13-14, 17 and 25 under Section 103(a) as obvious over Dailey in view of Daggett et al. U.S. Pat. No. 4,786,847. As an initial matter, in responding to this Office Action, Applicant reserves the right (and stands ready if necessary) to swear behind the Dailey reference – and thereby eliminate it as a reference. However, for at least the reasons set forth herein below, the Dailey reference, even if deemed prior art, would not render Applicant's claims unpatentable since Dailey lacks a number of the recited elements.

Applicant traverses the rejection of **claim 1** at **section 5** of the Office Action. Claim 1 is directed to a control processor (a single piece of computing hardware on a network – see control processor 2 in Fig. 1) that, in addition to executing a set of control blocks (according to well-known control processor architectures), executes a multivariable linear program that establishes process setpoints utilized by the set of control blocks in controlling a set of field devices associated with the industrial process. The multivariable linear program, executing at a relatively low execution priority in comparison to the execution priority of the set of control blocks, implements the dynamic model-based interactive control of the industrial process.

Dailey, on the other hand, discloses a flight controller including multiple channels having differing weights with regard to their use to control flight. Nowhere does Dailey suggest that the differing control signal channel priorities are in any way linked to execution priority of code sequences associated with the signal channels.

Dailey discloses foreground/background calculation of the same control values (at column 37, lines 20-28) that are output to control elements that effect flight control surfaces

that direct the flight path of a flying object. Applicant notes, however, the recited invention in claim 1 is not merely directed to the presence of multiple execution levels in a computer system. Rather, the invention recited in claim 1 embodies merging and prioritizing, within a single control processor, (1) implementing a model-based multivariable linear program (executed at a relatively lower execution priority) and (2) implementing a set of control blocks (executed at a relatively higher execution priority) that have output values that are transmitted to field devices of the industrial process. Dailey neither discloses nor suggests that the background task executed at a relatively low priority, renders process setpoints.

With regard to the Daggett reference, Applicant does not contest that control blocks have been previously executed, on a relatively higher priority basis, in the past within a control processor. However, neither Dailey nor Daggett suggests the combination of executing an embedded control task (including all the recited elements defining the functionality of the control task) at a relatively low level and executing a set of control blocks at a relatively high level *within a single control processor*. As an initial point, Dailey neither discloses nor suggests that the disclosed flight control system is to be implemented using control blocks (there is no suggestion in the prior art known to applicant that control blocks, used to control manufacturing systems, are used in the aeronautical flight control field to which Dailey is directed). Furthermore, neither the Dailey nor the Daggett reference discloses executing the recited embedded control task within the control processor that executes control blocks at a relatively high priority to render output values to field devices. Thus, the invention recited in claim 1 is patentable over the prior art.

For at least the above reasons, Applicant traverses the rejection of **claim 13 at section 8** of the Office Action. Though the claimed method differs from claim 1 in a number of ways, including the recitation of receiving (rather than transmitting) process variables, the claimed invention is similarly distinguished over the prior art teachings by the presence of the merged execution, on a single control processor, of distinct functional process control programs at different priority levels. An embedded multivariable control application is executed at a lower priority level, and a set of regulatory control blocks are executed at the relatively higher level. If the rejection of claim 13 is not withdrawn, Applicant requests specific identification of each of these two distinct types of executed software within a single

control processor – and/or the suggestion to modify a prior art control processor (running only the control blocks) to include these two specific types of software executed at differing priority levels.

Applicant traverses the rejection of **claims 2 and 14** in **section 6** of the Office Action. Claims 2 and 14 depend from and include all the recited elements of claims 1 and 13, respectively. Thus, for at least the reasons set forth above for claims 1 and 13, claims 2 and 14 are patentable over the prior art. Furthermore, the "supervisory control" discussed within the Daggett reference concerns a second computer (connected via a local area network) and thus does not meet the requirement of being executed within the control processor. "Supervisory program execution" to the extent understood by Applicant, does not refer to the recited "supervisory control blocks" that execute within the control processor. Applicant further traverses the rejection of claims 2 and 14 since there is no suggestion to incorporate the regulatory/supervisory control block-based process control system architecture of these claims into the flight control system described in Dailey – that makes no reference whatsoever to control blocks.

Applicant traverses the rejection of **claims 5 and 17** in **section 7** of the Office Action. Claims 5 and 17 depend from and include all the recited elements of claims 2 and 14, respectively. Thus, for at least the reasons set forth above for claims 1, 2, 13 and 14, claims 5 and 17 are patentable over the prior art. Furthermore, the matrices disclosed in the Dailey patent do not constitute a multivariable loop (MVL) block. The specification describes the MVL block at page 9 of the specification as follows:

> A multivariable loop (MVL) block 132 applies input variable values obtained from a number of sources to a control equation/program incorporated within the MVL block 132 to render a manipulated variable (MV) supervisory set point that is written to the regulatory control block 130. In the exemplary embodiment of a multivariable controller embedded within a control processor, the MVL block 132 receives as its inputs a setpoint value (generated by the embedded linear programming optimizer, by a non-embedded supervisory control program, or manually entered by a process operator) , a controlled variable (CV) from the input block 126, and a feedforward variable (FV) from the input block 128.

In the event that this rejection is not withdrawn, Applicant requests an explanation of how the matrices described in Dailey constitute the MVL block, defined in the specification and recited in claims 5 and 17, that supplies an input value to a regulatory control block.

Applicant traverses the rejection of **claim 25** in **section 9** of the Office Action. Claim 25 is similar to the other rejected independent claims. Claim 25 recites an industrial process control computer including multiple operating levels. At a background (interruptible, lower priority) level, the process control computer executes a multivariable process control application that includes instructions for implementing a multivariable linear program that generates a set of values corresponding to process control variable setpoints. At a foreground (interrupt driven, higher priority) level, the process control computer executes a set of control blocks. The set of control blocks include program instructions for receiving and storing a set of process variable values representing the state of a controlled process.

The elements of claim 25 have been distinguished from Dailey herein above, and those comments (e.g., distinguishing signal channels and executed program sequences) are incorporated by reference. Dailey does not disclose or suggest a "control block" based control system. Furthermore, there is no suggestion in either Dailey or Daggett that such control blocks can/should be used to carry out the flight control system described in Dailey.

More importantly neither Dailey nor Daggett suggest the execution of *both* a multivariable linear program and control blocks within a single process control computer. Dailey, at column 37, lines 20-28, does recite foreground/background execution of control calculations. However, Dailey does not teach or suggest that a multivariable process control application executes in the background that renders process control variable setpoints, and a set of control blocks execute in the foreground that receive and store process variable values representing the state of the controlled process. In the event that the rejection of claim 25 is not withdrawn, Applicant requests specific identification of these differing types of instruction sequences/process control constructs within the cited references as well as the suggestion to combine the teachings of Dailey and Daggett to render such a combination.

Applicant traverses the rejection of **claims 3-4 and 15-16** in **sections 10-11** of the Office Action as obvious over Dailey in view of Daggett et al. and Morshedi et al. U.S. Pat.

No. 5,481,716. As an initial matter, in responding to this Office Action, Applicant reserves the right (and stands ready if necessary) to swear behind the Dailey reference – and thereby eliminate it as a reference. However, for at least the reasons set forth herein below, the Dailey reference, even if deemed prior art, would not render Applicant's claims unpatentable since Dailey and the other cited references, as explained previously herein above, lack a number of the recited elements in the claims from which claims 3-4 and 15-16 depend.

Applicant traverses the rejection of **claims 3 and 15 in section 10** of the Office Action. Claims 3 and 15 depend from and include all the recited elements of claims 2 and 14, respectively. Thus, for at least the reasons set forth above for claims 1, 2, 13 and 14, claims 3 and 15 are patentable over the prior art. Claims 3 and 15, include the further element/step of a multivariable control (MVC) block that facilitates communicating data between the control processor and a workstation. Claim 15 calls for downloading the data from the workstation to a database accessed by the MVC that executes on the control processor. As an initial matter, Applicant notes *none* of the cited references discloses the MVC block (described at page 9 of Applicant's specification). Furthermore (with regard to claim 15), nowhere does Dailey suggest that its flight control system receives data (placed in a database), from a workstation, that is accessed by a multivariable control block – or the desirability/benefits of adding the particular described workstation/process controller data interface to the flight control system. In the event that the rejection of claims 3 and 15 is not withdrawn, Applicant requests identification of the MVC block in Dailey (if such exists) as well as the suggestion to modify Dailey's flight controller to include the recited functionality in claims 3 and 15.

Applicant traverses the rejection of **claims 4 and 16 in section 11** of the Office Action. Claims 4 and 16 depend from and include all the recited elements of claims 3 and 15, respectively. Thus for at least the reasons set forth above for claims 1-3 and 13-15, claims 4 and 16 are patentable over the prior art. Claims 4 and 16 additionally recite the element/step of the MVC block receiving/storing a process control model that is implemented by the embedded control task/control application. Nowhere in the cited portions of the Dailey reference is this element/step described. In fact, there is no description of how the matrices are populated in the Dailey flight controller. On the other hand, one would expect the flight

control model to be highly stable and not likely to be changed (for reasons of safety). Thus, one would not expect Dailey's flight controller to support the claimed functionality recited in claims 4 and 16 that enhance the alterability of a previously loaded control model while the control system is operating. For at least these reasons, there is no suggestion to create the inventions recited in claims 4 and 16.

Applicant traverses the rejection, in **sections** 12-21 of the Office Action, of **claims 6, 8-12, and 20-24** under Section 103(a) as obvious over Dailey in view of Daggett et al. and McManus et al. U.S. Pat. No. 4,788,647. As an initial matter, in responding to this Office Action, Applicant reserves the right (and stands ready if necessary) to swear behind the Dailey reference – and thereby eliminate it as a reference. However, for at least the reasons set forth herein below, the Dailey reference, even if deemed prior art, would not render Applicant's claims unpatentable since Dailey and the other cited references, as explained previously herein above, lack a number of the recited elements in the claims from which claims 6, 8-12 and 20-24 depend.

Applicant traverses the rejection of **claims 6 and 18** in **section 12** of the Office Action. Claims 6 and 18 depend from, and include the elements of, claims 5 and 17. Thus, for at least the reasons set forth above for claims 1, 2, 5, 13, 14 and 17, claims 6 and 18 are patentable over the prior art. Claims 6 and 18 recite the additional element/step of a PID block. Though Applicant agrees that McManus (and indeed many prior art systems) discloses a PID block, Applicant asserts that the modification asserted by the Office Action is neither suggested nor desirable in Dailey's flight controller. In fact, the disclosure/invention described in Dailey appears to take the place of a PID control block. Thus, there is no suggestion to modify the Dailey flight controller to include a PID control block. In the event this rejection is not withdrawn, Applicant requests an explanation of why (and how) one skilled in the art would be motivated to modify the flight controller disclosed in Dailey to include the recited PID control block.

Applicant traverses the rejection of **claim 8** in **section 13** of the Office Action. Claim 8 depends from, and includes all the elements of, claim 1. Thus, for at least the reasons set

forth above for claim 1, claim 8 is patentable over the prior art. Claim 8 recites a repetition cycle parameter that specifies a repetition period for the embedded control task recited in claim 1. Claim 8 further defines the industrial control processor architecture recited in claim 1 by adding an element of configurability to the repetition period of the embedded control task. The McManus reference discloses a configurable repetition period for a "power calculation task." The Office Action does not assert that this power calculation task has anything to do with the claimed "embedded control task" nor does the Office Action identify where, in the cited references, teachings suggest that such a configurable parameter should be incorporated into the Dailey control system. Such a modification to Dailey cannot be suggested by the McManus reference since the embedded control task does not even exist in Dailey.

In summary, the Office Action asserts, but does not explain where the prior art suggests modifying the Dailey flight controller to include an embedded control task having a configurable repetition period. However, the Dailey reference does not even disclose the embedded control task and the configurable repetition period in McManus merely relates to a power calculation task. Applicant requests identification of the apparently absent teachings in the prior art in the event that the rejection of claim 8 is not withdrawn.

Applicant traverses the rejection of **claim 9** in **section 14** of the Office Action. Claim 9 depends from, and includes all the elements of, claim 8. Thus, for at least the reasons set forth above for claims 1 and 8, claim 9 is patentable over the prior art. Claim 9 recites the additional element of a supervisory control block that controls restarting a repetition cycle of the embedded task in accordance with the repetition period parameter. While McManus, by necessity, includes some form of scheduling entity that controls the repeated "power calculation task," nowhere does McManus disclose that this function is carried out by a supervisory control block that executes within the control processor.

Applicant traverses the rejection of **claim 10** in **section 15** of the Office Action. Claim 10 depends from, and includes all the elements of, claim 1. Thus, for at least the reasons set forth above for claim 1, claim 10 is patentable over the prior art. Claim 10 recites the additional element of a block processing cycle parameter that specifies a repetition period

for executing the set of control blocks. The prior art however, fails to suggest modification of the Dailey reference (which does not even disclose control blocks) to include a parameter designating a block execution cycle repetition period.

Applicant, as an initial matter, traverses the assertion in the Office Action that a control system, by necessity includes control blocks. Many control systems do indeed incorporate a control block architecture. However, others, including the flight controller of the Dailey patent, do not include executable control blocks. Therefore, in view of the absence of a suggestion in the prior art to modify the Dailey flight controller to execute control blocks, the invention recited in claim 10, including a parameter defining a repetition period for executing the set of control blocks, cannot be obvious over the cited references.

Applicant traverses the rejection of **claim 11** in **section 16** of the Office Action. Claim 11 depends from, and includes all the elements of, claim 10. Thus, for at least the reasons set forth above for claims 1 and 10, claim 11 is patentable over the prior art. Claim 11 recites a repetition cycle parameter specifying a period for restarting a cycle of the embedded control task. As mentioned previously herein above, the Dailey reference does not even disclose an embedded control task. Furthermore, the repetition cycle recited in McManus concerns a power calculation task. Thus, combining Dailey and McManus, at best, would render a periodic calculation of an output value according to a repetition period. Nowhere does the prior art suggest a parameter for designating the repetition period of the embedded control task comprising a multivariable linear program that supplied setpoints for controlling an industrial process. Finally, it is noted that the Office Action does not appear to distinguish between the control block execution period and the embedded task execution period. The specification and claims make clear distinctions between these two periods and are not interchangeable.

Applicant traverses the rejection of **claims 12 and 24** in **section 17** of the Office Action. Claims 12 and 24 depend from, and include all the elements of, claims 11 and 13, respectively. Thus, for at least the reasons set forth above for claims 1, 10 and 11, claim 12 is also patentable, and claim 24 is patentable for at least the reasons set forth above with regard to claim 13. Claims 12 and 24 include the further specification that the embedded task

repetition period exceeds the control block repetition period. The cited portions of the McManus patent neither disclose nor suggest these two periods, and therefore cannot render claims 12 and 24 obvious.

Applicant traverses the rejection of **claim 20** in **section 18** of the Office Action. Claim 20 depends from, and includes all the elements of, claim 13. Thus, for at least the reasons set forth above for claim 13, claim 20 is patentable. Claim 20 further specifies maintaining a repetition cycle parameter specifying a period for restarting a cycle of the embedded task. For at least the reasons set forth above regarding claim 8 (reciting a similar set of elements), claim 20 is also patentable.

Applicant traverses the rejection of **claim 21** in **section 19** of the Office Action. Claim 21 depends from, and includes all of the elements of, claim 20. Thus, for at least the reasons set forth above for claims 13 and 20, claim 21 is patentable. Claim 21 further specifies determining, by a supervisory control block, when a next repetition period of the embedded task is to commence based upon the repetition cycle parameter. For at least the reasons set forth above regarding claim 9 (reciting a similar set of elements), claim 21 is also patentable.

Applicant traverses the rejection of **claim 22** in **section 20** of the Office Action. Claim 22 depends from, and includes all the elements of, claim 13. Thus, for at least the reasons set forth above for claim 13, claim 22 is patentable. Claim 22 further specifies a step of maintaining a block processing cycle parameter specifying a repetition period for commencing a cycle of processing the set of control blocks. For at least the reasons set forth above regarding claim 10 (reciting similar elements), claim 22 is patentable over the prior art.

Applicant traverses the rejection of **claim 23** in **section 21** of the Office Action for at least the reasons set forth above with regard to claim 20 (the previously rejected claim upon which the Office Action bases its rejection of claim 23). Applicant also traverses the rejection of claim 23 in view of the reasons set forth above with regard to claim 11 (including similar claim elements).

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Applicant traverses the rejection of **claims 7 and 19** in **section 22** of the Office Action under Section 103(a) as obvious over the Dailey in view of Daggett et al. and Westergren et al. U.S. Pat. No. 5,423,076. Claims 7 and 19 depend from, and include all the elements of, claims 5 and 17. Thus, for at least the reasons set forth above with regard to claims 1, 2, 5, 13, 14 and 17, claims 7 and 19 are patentable. Furthermore, while Westergren does indeed disclose a ratio block, there is no suggestion to place such a regulatory control block within the flight controller described in the Dailey reference. Neither Dailey nor Daggett et al. suggest a need to incorporate a ratio block into their specific examples of control systems. Westergren does not suggest that its ratio block is applicable in either the Dailey flight control system or the system disclosed in Daggett et al.

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Conclusion

The application is considered in good and proper form for allowance, and the Examiner is respectfully requested to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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